REMARKS/ARGUMENTS

Claims 1-49 stand rejected in the outstanding Official Action. Claims 1, 4, 6, 7, 17, 19, 20, 23, 32, 35, 38, 40, 41, 44 and 45 have been amended and therefore claims 1-49 remain in this application.

The Examiner's withdrawal of the previous rejections under 35 USC §101 and §102 is very much appreciated.

Current claims 1-7, 12-23 and 28-45 stand rejected under 35 USC §103 as unpatentable over Gupte (U.S. Patent 5,903,475) in view of Holstine ("Developing an EDA Vendor-Independent ASIC System for VHDL" by Bob Holstine and Greg Haynes).

The Examiner's admission at the bottom page 5 of the outstanding Official Action that "Gupte does not expressly teach recording input signals to and output signals from said subsystem circuit in response to changes in at least one of said input signals and said output signals" is very much appreciated.

Applicants have also amended independent claim 1 (and the other independent claims) to recite the additional method step (structure and/or logic in the other independent claims) of "generating, in dependence upon said recorded signals, a plurality of non cycle-based sampling rules defining at least one of times at which said output signals should be sampled and ranges of times within which said output signals should change."

Neither Gupte nor Holstine disclose this features which specifies that a plurality of non cycle-based sampling rules is generated in dependence upon the recorded signals and these rules defining at least one of the times at which the output signals should be sampled and ranges of times within which the output signals should change. This modification to the claim avoids any

indefiniteness as to what is meant in the claim by non cycle-based sampling rules and is incorporated from page 7, lines 12-17 in the present application. This is responsive to the Examiner's earlier inquiry with regard to the phrase "without requiring a periodic sampling reference" and obviates any further objection thereto.

On page 6 of the Official Action, the Examiner suggests that Holstine teaches a feature of the present claim 1 (and other independent claims) of "recording input signals to and output signals from a subsystem circuit in response to changes in at least one of the input signals and the output signals." Firstly, the Examiner does not fully quote the last portion of claim 1 which reads "recording input signals to and output signals from a subsystem circuit in response to changes in at least one of the input signals and the output signals whilst performing said test sequence of data processing operations." There has been no allegation that the fulled defined feature of claim 1 is present ineither Gupte or Holstine.

Secondly, the Examiner appears not to appreciate that Gupte discloses a system in which a set of golden vectors are captured during system simulation and the outputs generated by an ASIC during stand-alone simulation are compared to the golden vectors to test for correct operation of that ASIC (see Gupte column 2, lines 6-22). Thus, Gupte describes a simple **cycle-based** approach in which test vectors are replayed and responses recorded. Such systems have been acknowledged as well known in the present specification (see page 4, lines 12 and 13).

Claim 1 positively recites the use of a plurality of "**non cycle-based** sampling rules" (emphasis added) which provides greater flexibility as to when the sampling of signals is to occur and to determine what behavior is acceptable in terms of indicating correct operation. This flexibility simply cannot be provided by the cycle-based system disclosed in Gupte.

While the Examiner suggests in the second paragraph on page 6 that "Holstine and Gupte are analogous art because both are drawn to circuit simulation," he does not address the fact that neither Gupte nor Holstine disclose or suggest testing for operation of a data processing apparatus by generating a plurality of **non cycle-based sampling rules** as specified by amended claim 1. Thus, even if Gupte and Holstine were combined as suggested by the Examiner, they would not disclose or render obvious the subject matter of claim 1 and the other independent claims.

On page 7 of the Official Action, the Examiner contends that Gupte discloses the feature of claim 4 (and similar other dependent claims). However, there is no indication that Gupte discloses a "time window" as specified in claim 4. Rather, Gupte discloses sampling instance, i.e., at specific times, at which the output signals are sampled. In order to clarify the distinction between Gupte's sampling instant and the claim 4 sampling during a time window, claim 4 has been modified. This amendment renders it clear that the periodic strobe signal of Gupte which is used to sample output vectors is not analogous to Applicants' output signal time window. The basis for the amendments to claim 4 (and other claims in this regard) is found in the description of Figure 5 on pages 9 and 10 of the specification.

On page 8 of the Official Action, the Examiner contends that Gupte discloses the subject matter of claim 6 (and other similar claims in the application). The Examiner contends that the periodic signal of Gupte which is used to trigger periodic sampling of the output signals is the counterpart of a strobe signal of claim 6. Applicants have clarified claim 6 to indicate that the strobe signal is an output signal "other than a repetitive clock signal." Support in Applicants' specification is found on page 7 (sixth line from the bottom in reference to Figure 3 which refers

to "generation of repetitive clocks"). One of ordinary skill in the art reading Gupte will understand that the strobe signal in the Gupte system is not in fact a strobe signal according to the present invention. The discussion of Figure 5 on pages 9 and 10 provides exemplary embodiments in which the strobe signal is the rising edge of a read enable signal.

In view of the above, there is simply no support in the Gupte/Holstine combination for a rejection of the subject matter of claims 1-7, 12-23 and 28-45 and any further rejection thereunder is respectfully traversed. Again, as noted before, there is no reason for combining the Gupte reference with the Holstine reference, but even if those references were combined, they would not render obvious the subject matter of Applicants' claims. Accordingly, any further rejection of claims 1-7, 12-23 and 28-45 under 35 USC §103 is respectfully traversed.

Claims 8-11, 24-27 and 46-49 stand rejected under 35 USC §103 as unpatentable over the Gupte/Holstine combination, further in view of Synopsys ("SourceModel User's Manual for VHDL"). The Examiner's admission that neither "Gupte nor Holstine expressly teach a rule that include a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation" is very much appreciated. Inasmuch as this rejection relies upon the Gupte/Holstine combination, the above comments distinguishing independent claim 1, from which claims 8-11 ultimately depend, independent claim 19, from which dependent claims 24-27 ultimately depend and independent claim 44, from which dependent claims 46-49 ultimately depend, with respect to the generating a "plurality of non cycle-based sampling rules" are herein incorporated by reference. Accordingly, it is unnecessary to further elaborate on the distinctions of claims 8-11, 24-27 and 46-49 over the

Gupte/Holstine/Synopsis combination and any further rejection thereunder is respectfully traversed.

Having responded to all objections and rejections set forth in the outstanding Official Action, it is submitted that claims 1-49 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is respectfully requested to contact Applicants' undersigned representative.

Respectfully submitted,

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